Electrical Stability of Hexagonal a-Si:H TFTs

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***Abstract*—In this letter, we study the current–temperature-stress-induced electrical instability of single and multiple hexagonal (HEX) hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) connected in parallel. The influence of the threshold voltage shift of a single HEX TFT on the overall electrical performance of multiple HEX TFTs is discussed. The results indicate that a-Si:H HEX TFTs have an improved electrical stability and a threshold voltage shift linear dependence on a number of connected HEX-TFT units.**

***Index Terms*—Amorphous silicon, current–temperature stress (CTS), hexagonal thin-film transistor (HEX TFT), parallel-connected transistors, threshold voltage (V_{th}).**

I. Introduction

Hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) have been extensively used as pixel circuits for large-area flat-panel displays and X-ray imagers due to excellent spatial uniformity and low fabrication cost [1], [2]. To use such devices for active-matrix organic light-emitting diodes (AM-OLEDs) and various analog amplifiers and switches, a higher drain current and a better electrical stability under prolonged bias stress are required [3], [4]. For a given channel length of a standard TFT, a higher drain current can be achieved by increasing the TFT channel width using comb-shaped [5] or fork-shaped [6] electrodes. It is known that TFTs with asymmetric source–drain electrode have a better electrical stability compared to a standard TFT for the same channel width to length (W/L) ratio at a proper bias condition [7].

We proposed Corbino and hexagonal (HEX) a-Si:H TFTs to achieve a large channel width without scarifying electrical stability [8], [9]. Such device designs provide a larger pixel aperture ratio compared to a standard TFT for a given channel width. Moreover, the a-Si:H HEX-TFT current level can be adjusted to a desirable value by connecting a number of HEX TFTs in parallel. To assess the potential of HEX TFTs connected in parallel for future flat-panel displays, it is essential to evaluate their electrical stability. In this letter, we report the detailed studies of the current–temperature stress (CTS)-induced electrical instability of a single and multiple HEX TFT.

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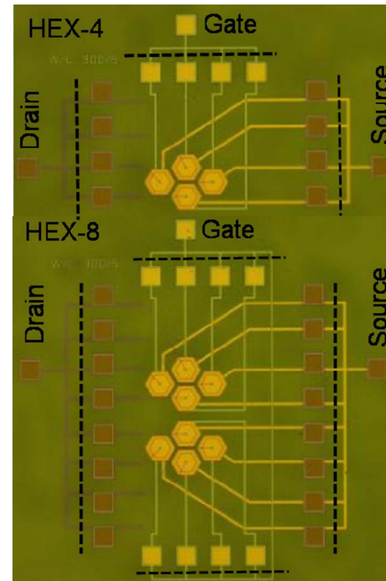

Fig. 1. Photographs of the fabricated multiple HEX TFTs (e.g., HEX-4 and HEX-8 TFTs). Drain to inner electrode and source to outer electrode. Dashed lines show the cutting line to separate and measure individual HEX-TFT unit.

We first measured the ΔV_{th} of single HEX TFTs at an elevated temperature (80 °C) and then investigated their contribution to the overall ΔV_{th} of multiple HEX TFTs.

II. Experiments

Inverted stagger a-Si:H HEX TFTs were fabricated with five-photomask process used in the processing of the active-matrix liquid crystal displays. All multiple HEX TFTs were based on identical single HEX TFTs. Gate, drain, and source electrodes are connected in parallel, respectively (Fig. 1). Detailed process steps can be found in the previous publication [9].

A series of CTS measurements of the single and multiple HEX TFTs was performed by using a semiconductor parameter analyzer (HP 4156A) under an accelerated stress condition by setting the stress temperature (T_{STR}) at 80 °C. During the CTS measurements, we connected the gate and drain biases (inner electrode) together and continuously applied the current through the drain to the TFTs. The source (outer electrode) of the TFT was grounded. Thus, the TFTs operate in the saturation regime. We applied different drain current values, depending on the channel width, to maintain the same stress current density $(J_{\mathrm{STR}} = 1667\ \mathrm{A/cm^2})$ that corresponds to the OLED luminance of 10 000 cd/m^2 for an emission efficiency of 3.0 cd/A and a pixel size of $300 \times 100\ \mu\mathrm{m}^2$ [9]. For example, drain currents of 50, 100, and 167 μA were applied to HEX-1 $(W/L = 300/5)$, HEX-2 $(W/L = 600/5)$, and standard $(W/L = 1000/6)$ a-Si:H TFTs, respectively. The

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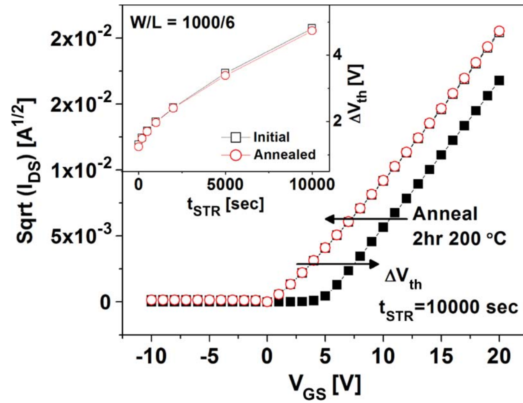

Fig. 2. Recovery of the CTS-induced stress after thermal annealing. The transfer characteristic is restored to the initial state after the thermal annealing at 200 °C for 2 h. The inset shows the threshold voltage shift ($\Delta V_{\rm th}$) as a function of stress time ($t_{\rm STR}$). Squares and circles represent the CTS results of the initial and annealed TFTs, respectively.

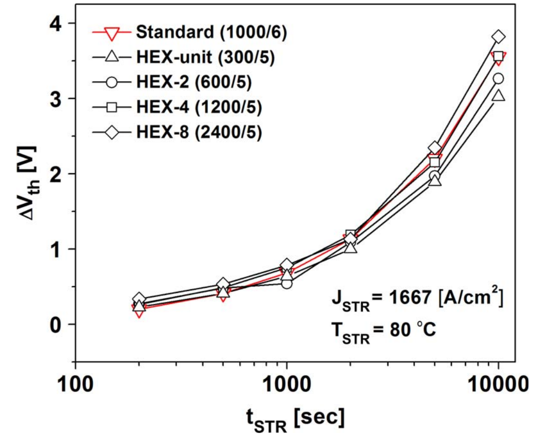

Fig. 3. Threshold voltage shifts ($\Delta V_{\rm th}$) of the single HEX-TFT unit, HEX-2, HEX-4, and HEX-8 TFT as a function of stress time ($t_{\rm STR}$) in a semilog scale. The applied current density ($J_{\rm STR}$) and the stress temperature ($T_{\rm STR}$) are 1667 $\rm A/cm^2$ and 80 °C, respectively. The result of the standard TFT is shown for comparison.

total stress time ($t_{\rm STR}$) was 10 000 s, and we only interrupted the applied stress for 60 s to measure the transfer characteristics. Using the same condition, we also measured independently all HEX-TFT basic units by cutting the parallel connection lines (Fig. 1). A standard TFT ($W/L = 1000/6$) was measured as well for comparison. We performed thermal annealing at 200 °C for 2 h to ensure the consistent initial properties of the a-Si:H TFTs before each CTS measurement. Fig. 2 shows that the CTS-induced stress could be fully recovered after each thermal annealing. Using the effective channel width calculated by Lee *et al.* [9], we extracted the threshold voltages using the maximum slope method over the stress time. The threshold voltage shift ($\Delta V_{\rm th}$) is defined as follows:

$$\Delta V_{\rm th}(t) = V_{\rm th}(t = t_{\rm STR}) - V_{\rm th}(t = 0). \tag{1}$$

III. Results and Discussions

Fig. 3 shows the $\Delta V_{\rm th}$ variation as a function of stress time ($t_{\rm STR}$) for different TFTs studied in this letter. The $\Delta V_{\rm th}$ values of HEX-2 ($W/L = 600/5$), HEX-4 ($W/L = 1200/5$), and HEX-8 ($W/L = 2400/5$) are 3.26, 3.56, and 3.82 V, respectively. $\Delta V_{\rm th}$ increases with W/L ratio: larger width results in larger $\Delta V_{\rm th}$ for a given channel length ($L = 5$ μm). Because HEX-4 with even higher W/L ratio exhibited similar $\Delta V_{\rm th}$ to standard TFT ($W/L = 1000/6; \Delta V_{\rm th} = 3.55$ V), parallel-connected multiple HEX TFTs appear to have a better electrical stability (less $\Delta V_{\rm th}$) for the same W/L ratio compared to a standard TFT. Field-effect mobility ($\mu_{\rm eff}$) was also extracted from the transfer characteristics. The amounts of $\mu_{\rm eff}$ change ($\Delta\mu_{\rm eff}$) after the CTS measurement for the standard TFT, HEX-2, HEX-4, and HEX-8 are 0.06, 0.07, 0.09, and 0.12 $\rm cm^2/(V \cdot s)$, respectively.

The influence of the $\Delta V_{\rm th}$ of a single HEX TFT on the $\Delta V_{\rm th}$ of multiple HEX TFTs was also investigated. The $\Delta V_{\rm th}$ of all single HEX TFTs for both HEX-4 and HEX-8 is 3.04 V $\pm$ 0.06. No specific single HEX TFT dominates the overall circuit electrical instability due to adequate a-Si:H TFT process spatial

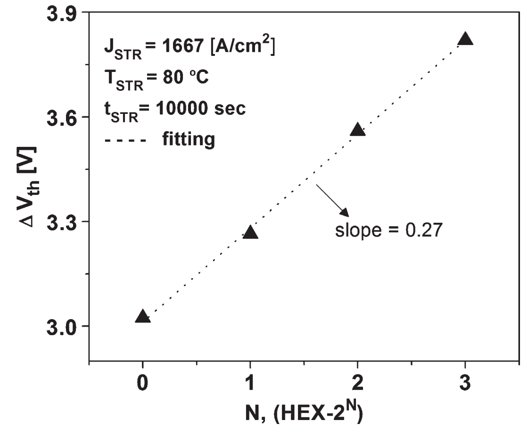

Fig. 4. CTS-induced threshold voltage shift ($\Delta V_{\rm th}$) as a function of integer N of HEX-2^N.

uniformity. We also estimated the $\Delta V_{\rm th}$ of parallel-connected multiple HEX TFTs based on their unit device. The $\Delta V_{\rm th}$ of HEX-2^N TFT (N integer) can be described by $\Delta V_{{\rm th}_N} = \Delta V_{{\rm th}_u} + N \times 0.27$, where $\Delta V_{{\rm th}_u}$ is the $\Delta V_{\rm th}$ of unit HEX TFT and N is from HEX-2^N TFT (Fig. 4). The linear relation between $\Delta V_{\rm th}$ and number of unit TFTs can be explained as follows: For this specific experimental bias condition, $\Delta V_{\rm th}$ is dominated by a combination of defect creation or/and charge trapping [10]. Indeed, Fig. 3 shows a power-law dependence between $\Delta V_{\rm th}$ and the stress time ($t_{\rm STR}$). We observed that $\Delta V_{\rm th} \propto t_{\rm STR}^{\beta}$, and β is extracted to be 0.65 $\pm$ 0.02. For a-Si:H TFT, the total channel charge ($Q_{\rm ch}$) in the saturation region is given by [11]

$$Q_{\rm ch} = \frac{2}{3} C_G \cdot W \cdot L(V_{\rm GS} - V_{\rm th}) \tag{2}$$

where C_G is the gate capacitance per unit area, W is the channel width, L is the channel length, and $V_{\rm GS}$ is the gate-source bias. The channel width increases with the number of parallel-connected HEX TFTs, and so does the total channel charge.

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For larger $Q_{\rm ch}$, we expect that a larger number of carriers are available for either to be trapped at the silicon nitride/ a-Si:H interface or/and to participate in the breaking of Si–Si weak bonds to create charged Si defects. Both mechanisms will produce $\Delta V_{\rm th}$ that is proportional to the number of trapped charges. In other words, a larger number of trapped charges will result in a larger threshold voltage shift in agreement with the experiments.

IV. Conclusion

We have studied the electrical instability of single and multiple a-Si:H HEX TFTs under CTS. Multiple HEX TFTs show a better electrical stability compared to the standard TFT for similar W/L ratio. It has been found that one specific HEX unit in the multiple HEX TFTs does not dominate or/and affect the overall TFT electrical instability. Furthermore, we have established a relationship between the threshold voltage shift and the number of units in the multiple HEX TFT. These new devices have promising characteristics for AM-OLEDs and other flat-panel displays.

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